

SPECIFICATION

TITLE OF THE INVENTION

5 SPST SWITCH, SPDT SWITCH AND MPMT SWITCH

TECHNICAL FIELD

The present invention relates to a single-pole single-throw (SPST) switch, a single-pole double-throw (SPDT) switch 10 and a multiple-pole multiple-throw (MPMT) switch for controlling propagation of a high frequency signal.

BACKGROUND ART

FIG. 1 is a circuit diagram showing a conventional SPDT 15 switch shown in "High-power microwave transmit-receive switch with series and shunt GaAs FETs", IEICE Trans. ELECTRON, Feb. 1992.

The SPDT switch as shown in FIG. 1 has an input terminal 1a, output terminal 1b, output terminal 1c, FET (field-effect 20 transistor) 2a, FET 2b, inductor 3a, inductor 3b, line 4 and ground 5. The FET 2a has its drain connected to the input terminal 1a, and its source connected to the output terminal 1c. The inductor 3a has its first terminal connected to the input 25 terminal 1a, and its second terminal connected to the output terminal 1c. The line 4 has its first terminal connected to the input terminal 1a, and its second terminal connected to the output terminal 1b. The FET 2b has its drain connected to the output terminal 1b, and its source connected to the ground 5. The inductor 3b has its first terminal connected to the output 30 terminal 1b, and its second terminal connected to the ground

5.

Next the operation will be described.

In FIG. 1, the FET 2a and FET 2b operate as switches for switching between the ON state and OFF state in response to a 5 voltage applied to their gates. When a gate voltage with the same potential as the drain voltage and source voltage is applied to the gate of the FET 2a, the FET 2a is brought into the ON state and exhibits a resistance property. On the other hand, when a voltage less than the pinch-off voltage is applied to 10 the gate of the FET 2a, the FET 2a is brought into the OFF state and exhibits a capacitance property. The FET 2b operates in the same manner.

FIG. 2 is an equivalent circuit diagram when the FET 2a and FET 2b in FIG. 1 are brought into the OFF state. As shown 15 in FIG. 2, when the FET 2a is brought into the OFF state, a state arises in which a parallel connection of an OFF capacitance 9 and an OFF resistance 10 is connected in series with a parasitic inductor 8 between the drain or source 6a and the source or drain 6b of the FET 2a. The same state arises when the FET 2b is brought 20 into the OFF state.

FIG. 3 is an equivalent circuit diagram when the FET 2a and FET 2b in FIG. 1 are brought into an ON state. As shown in FIG. 3, when the FET 2a is brought into the ON state, a state arises in which the ON resistance 7 and parasitic inductor 8 25 are connected in series between the drain or source 6a and the source or drain 6b of the FET 2a. The same state arises when the FET 2b is brought into the ON state.

In FIG. 1, consider the case where the FET 2a and FET 2b are brought into the OFF state, that is, when the equivalent 30 circuit diagram of the FET 2a and FET 2b is FIG. 2. At the

frequency  $f_1$  used by the SPDT switch, when the reactance component of the parasitic inductor 8 is small enough as compared with the reactance component of the OFF capacitance 9, and the OFF resistance 10 is sufficiently large, and when the 5 relationship holds of  $f_1 = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 9\ of\ FET\ 2a) \times (inductance\ of\ inductor\ 3a)} = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 9\ of\ FET\ 2b) \times (inductance\ of\ inductor\ 3b)}$ , the impedance of the output terminal 1b seen from the input terminal 1a becomes low, and the impedance of the output terminal 10 1c seen from the input terminal 1a becomes high. In this case, the high frequency signal input through the input terminal 1a is fed to the output terminal 1b.

In addition, consider the case where the FET 2a and FET 2b are brought into the ON state in FIG. 1, that is, when the 15 equivalent circuit diagram of the FET 2a and FET 2b is FIG. 3. In this case, the impedance of the output terminal 1b seen from the input terminal 1a becomes high, and the impedance of the output terminal 1c seen from the input terminal 1a becomes low. Thus, the high frequency signal input through the input terminal 20 1a is fed to the output terminal 1c.

With the foregoing configuration, the conventional SPDT switch has the following problem. When the gate width of the FET 2a and FET 2b is increased to achieve high withstanding power, the reactance component of the parasitic inductor 8 comes to 25 be not negligible as compared with the reactance component of the OFF capacitance 9, and the OFF resistance 10 becomes small. Accordingly, when the FET 2a and FET 2b are brought into the OFF state, the propagation loss of the high frequency signal propagating from the input terminal 1a to the output terminal 30 1b increases, which presents a problem of reducing the isolation

of the high frequency signal from the input terminal 1a to the output terminal 1c.

Although the conventional technique is described by way of example of the SPDT switch, an SPST switch or MPMT switch 5 has the same problem.

The present invention is implemented to solve the foregoing problem. Therefore it is an object of the present invention to provide an SPST switch, SPDT switch and MPMT switch having characteristics of being able to achieve high withstanding power, 10 to reduce propagation loss of the high frequency signal, and to prevent the reduction in the isolation.

#### DISCLOSURE OF THE INVENTION

According to one aspect of the present invention, there 15 is provided an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal and an output terminal, the SPST switch comprising: a plurality of first field-effect transistor switches connected in parallel, each of which includes a 20 field-effect transistor having its drain and source connected in parallel with an inductor, wherein each of the field-effect transistors has its ON state and OFF state changed by a voltage applied to a gate of each of the field-effect transistors, and each of the field-effect transistors has its OFF capacitance 25 cause parallel resonance with the inductor connected at a frequency of the high frequency signal.

According to the present invention, an advantage is obtained of being able to achieve high withstanding power, and to reduce the propagation loss of the high frequency signal from 30 the input terminal to the output terminal, and to prevent

reduction in the isolation of the high frequency signal from the input terminal to the output terminal.

#### BRIEF DESCRIPTION OF THE DRAWINGS

5 FIG. 1 is a circuit diagram showing a conventional SPDT switch;

FIG. 2 is an equivalent circuit diagram when field-effect transistors in FIG. 1 are brought into the OFF state;

10 FIG. 3 is an equivalent circuit diagram when the field-effect transistors in FIG. 1 are brought into the ON state;

FIG. 4 is a circuit diagram showing a configuration of an SPST switch of an embodiment 1 in accordance with the present invention;

15 FIG. 5 is an equivalent circuit diagram when field-effect transistors in FIG. 4 are brought into the OFF state;

FIG. 6 is an equivalent circuit diagram when the field-effect transistors in FIG. 4 are brought into the ON state;

20 FIG. 7 is a circuit diagram showing a configuration of an SPST switch of an embodiment 2 in accordance with the present invention;

FIG. 8 is an equivalent circuit diagram when field-effect transistors in FIG. 7 are brought into the OFF state;

FIG. 9 is an equivalent circuit diagram when the field-effect transistors in FIG. 7 are brought into the ON state;

25 FIG. 10 is a circuit diagram showing a configuration of an SPST switch of an embodiment 3 in accordance with the present invention;

FIG. 11 is an equivalent circuit diagram when the field-effect transistor in FIG. 10 is brought into the OFF state;

30 FIG. 12 is an equivalent circuit diagram when the

field-effect transistor in FIG. 10 is brought into the ON state;

FIG. 13 is a circuit diagram showing a configuration of an SPST switch of an embodiment 4 in accordance with the present invention;

5 FIG. 14 is an equivalent circuit diagram when the field-effect transistor in FIG. 13 is brought into the OFF state;

FIG. 15 is an equivalent circuit diagram when the field-effect transistor in FIG. 13 is brought into the ON state;

10 FIG. 16 is a circuit diagram showing a configuration of an SPST switch of an embodiment 5 in accordance with the present invention;

FIG. 17 is an equivalent circuit diagram when field-effect transistors in FIG. 16 are brought into the OFF state;

15 FIG. 18 is an equivalent circuit diagram when the field-effect transistors in FIG. 16 are brought into the ON state;

FIG. 19 is a circuit diagram showing a configuration of an SPST switch of an embodiment 6 in accordance with the present invention;

20 FIG. 20 is an equivalent circuit diagram when field-effect transistors in FIG. 19 are brought into the OFF state;

FIG. 21 is an equivalent circuit diagram when the field-effect transistors in FIG. 19 are brought into the ON state;

25 FIG. 22 is a circuit diagram showing a configuration of an SPDT switch of an embodiment 7 in accordance with the present invention;

FIG. 23 is an equivalent circuit diagram when field-effect transistors in FIG. 22 are brought into the OFF state;

30 FIG. 24 is an equivalent circuit diagram when the

field-effect transistors in FIG. 22 are brought into the ON state;

FIG. 25 is a circuit diagram showing a configuration of an MPMT switch of an embodiment 8 in accordance with the present 5 invention; and

FIG. 26 is a table illustrating the operation of the MPMT switch of FIG. 25.

#### BEST MODE FOR CARRYING OUT THE INVENTION

10 The best mode for carrying out the invention will now be described with reference to the accompanying drawings to explain the present invention in more detail.

#### EMBODIMENT 1

15 FIG. 4 is a circuit diagram showing a configuration of an SPST switch of an embodiment 1 in accordance with the present invention. The SPST switch shown in FIG. 4 has an input terminal 11a, output terminal 11b, FET (field-effect transistor) 12a, FET 12b, inductor 13a and inductor 13b. The parallel connection of the FET 12a and inductor 13a constitutes a first FET switch 20 14a, and the parallel connection of the FET 12b and inductor 13b constitutes a first FET switch 14b. The FET switches 14a and 14b have their first terminals connected to the input terminal 11a, and their second terminals connected to the output terminal 11b. Thus, the first FET switch 14a is connected in 25 parallel with the first FET switch 14b in the present embodiment 1.

30 Connecting the two FETs 12a and 12b in parallel can halve their individual gate width to achieve the same withstanding power. Halving the individual gate width can make the reactance components of the parasitic inductors of the FETs 12a and 12b

small enough as compared with the reactance component of the OFF capacitance at the frequency  $f$  used by the SPST switch, and make the OFF resistance large enough.

Here, the drains of the FET 12a and FET 12b can be connected 5 to the input terminal 11a or output terminal 11b, and the sources of the FET 12a and FET 12b can be connected to the output terminal 11b or input terminal 11a.

Next the operation will be described.

In FIG. 4, the FET 2a and FET 2b operate as switches for 10 switching between the ON state and OFF state by the voltages applied to the gates.

FIG. 5 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 4 are brought into the OFF state. As shown in FIG. 5, when the FET 12a is brought into the OFF state, a 15 state arises in which the OFF capacitance 15a and OFF resistance 17a which are connected in parallel are connected in series with the parasitic inductor 16a, and when the FET 12b is brought into the OFF state, a state arises in which the OFF capacitance 15b and OFF resistance 17b which are connected in parallel are 20 connected in series with the parasitic inductor 16b.

At the frequency  $f$  used by the SPST switch, the reactance components of the parasitic inductors 16a and 16b are small enough as compared with the reactance components of the OFF capacitances 15a and 15b, and the OFF resistances 17a and 17b 25 are large enough. Thus, when  $f = 1/\sqrt{}$  (capacitance of OFF capacitance 15a)  $\times$  (inductance of inductor 13a)  $= 1/\sqrt{}$  (capacitance of OFF capacitance 15b)  $\times$  (inductance of inductor 13b), that is, when the inductor 13a that will cause parallel 30 resonance with the OFF capacitance 15a at the used frequency  $f$  is connected, and when the inductor 13b that will cause parallel

resonance with the OFF capacitance 15b at the used frequency f is connected, the impedance of the output terminal 11b seen from the input terminal 11a becomes high. In this case, the high frequency signal input through the input terminal 11a is not fed to the output terminal 11b, and the isolation does not reduce of the high frequency signal from the input terminal 11a to the output terminal 11b.

FIG. 6 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 4 are brought into the ON state. As shown in FIG. 6, when the FET 12a is brought into the ON state, a state arises in which the ON resistance 18a and parasitic inductor 16a are connected in series, and when the FET 12b is brought into the ON state, a state arises in which the ON resistance 18b and parasitic inductor 16b are connected in series.

In this case, since the first FET switches 14a and 14b are connected in parallel, the impedance of the output terminal 11b seen from the input terminal 11a becomes low. Thus, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b can be reduced.

In the present embodiment 1, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the input terminal 11a.

In addition, although the two first FET switches 14a and 14b are connected in parallel to halve the gate width of each

of the FETs 12a and 12b in the present embodiment 1, this is not essential. A configuration is also possible in which two or more first FET switches are connected in parallel to narrow the gate width in accordance with the number of the FETs.

5 As described above, the present embodiment 1 can halve the gate width for achieving the same withstanding power by connecting the first FET switches 14a and 14b in parallel, and can make, at the used frequency  $f$  of the SPST switch, the reactance components of the parasitic inductors 16a and 16b of 10 the FETs 12a and 12b small enough as compared with the reactance components of the OFF capacitances 15a and 15b, and make the OFF resistances 17a and 17b large enough. Thus, connecting the inductors 13a and 13b that will cause the parallel resonance with the OFF capacitances 15a and 15b offers an advantage of 15 being able to achieve the high withstanding voltage and prevent the reduction in the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b, and to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b.

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## EMBODIMENT 2

FIG. 7 is a circuit diagram showing a configuration of an SPST switch of an embodiment 2 in accordance with the present invention. As the SPST switch of the embodiment 1 shown in FIG. 25 4, the SPST switch shown in FIG. 7 has an input terminal 11a, output terminal 11b, FET 12a, FET 12b, inductor 13a and inductor 13b. The parallel connection of the FET 12a and inductor 13a constitutes a first FET switch 14a, and the parallel connection of the FET 12b and inductor 13b constitutes a first FET switch 30 14b. The embodiment 2, however, differs from the embodiment 1

in that the input terminal 11a and the output terminal 11b are connected directly, and in that the first FET switch 14a and first FET switch 14b have their first terminals connected to the input terminal 11a and output terminal 11b, and their second 5 terminals connected to the ground 19. Thus, in the present embodiment 2, the first FET switch 14a is connected in parallel with the first FET switch 14b.

Connecting the two FETs 12a and 12b in parallel can halve their individual gate width to achieve the same withstanding 10 power. Halving the individual gate width can make the reactance components of the parasitic inductors of the FETs 12a and 12b small enough as compared with the reactance component of the OFF capacitance at the frequency  $f$  used by the SPST switch, and make the OFF resistance large enough.

15 Here, the drains of the FET 12a and FET 12b can be connected to the input terminal 11a or the ground 19, and the sources of the FET 12a and FET 12b can be connected to the ground 19 or input terminal 11a.

Next the operation will be described.

20 In FIG. 7, the FET 2a and FET 2b operate as switches for switching between the ON state and OFF state by the voltages applied to the gates.

FIG. 8 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 7 are brought into the OFF state. As shown 25 in FIG. 8, when the FET 12a is brought into the OFF state, a state arises in which the OFF capacitance 15a and OFF resistance 17a which are connected in parallel are connected in series with the parasitic inductor 16a, and when the FET 12b is brought into the OFF state, a state arises in which the OFF capacitance 15b 30 and OFF resistance 17b which are connected in parallel are

connected in series with the parasitic inductor 16b.

In this case, at the frequency  $f$  used by the SPST switch, the reactance components of the parasitic inductors 16a and 16b are small enough as compared with the reactance components of the OFF capacitances 15a and 15b, and the OFF resistances 17a and 17b are large enough. Thus, when  $f = 1/\sqrt{}$  (capacitance of OFF capacitance 15a)  $\times$  (inductance of inductor 13a)  $= 1/\sqrt{}$  (capacitance of OFF capacitance 15b)  $\times$  (inductance of inductor 13b), that is, when the inductor 13a that will cause parallel resonance with the OFF capacitance 15a at the used frequency  $f$  is connected, and when the inductor 13b that will cause parallel resonance with the OFF capacitance 15b at the used frequency  $f$  is connected, the impedance of the ground 19 seen from the input terminal 11a becomes high. As a result, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal can be reduced.

FIG. 9 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 7 are brought into the ON state. As shown in FIG. 9, when the FET 12a is brought into the ON state, a state arises in which the ON resistance 18a and parasitic inductor 16a are connected in series, and when the FET 12b is brought into the ON state, a state arises in which the ON resistance 18b and parasitic inductor 16b are connected in series.

In this case, since the first FET switches 14a and 14b are connected in parallel, the impedance of the ground 19 seen from the input terminal 11a becomes low. Thus, the high frequency signal input through the input terminal 11a is propagated to the ground 19 without being fed to the output terminal 11b, and the isolation is not reduced of the high frequency signal from

the input terminal 11a to the output terminal 11b.

In the present embodiment 2, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the input terminal 11a.

In addition, although the two first FET switches 14a and 14b are connected in parallel to halve the gate width of each of the FETs 12a and 12b in the present embodiment 2, this is not essential. A configuration is also possible in which two or more first FET switches are connected in parallel to narrow the gate width in accordance with the number of the FETs.

As described above, the present embodiment 2 can halve the gate width for achieving the same withstanding power by connecting the first FET switches 14a and 14b in parallel, and can make, at the used frequency  $f$  of the SPST switch, the reactance components of the parasitic inductors 16a and 16b of the FETs 12a and 12b small enough as compared with the reactance components of the OFF capacitances 15a and 15b, and make the OFF resistances 17a and 17b large enough. Thus, connecting the inductors 13a and 13b that will cause the parallel resonance with the OFF capacitances 15a and 15b offers an advantage of being able to achieve the high withstanding voltage and to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b, and to prevent the reduction in the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b.

## EMBODIMENT 3

FIG. 10 is a circuit diagram showing a configuration of an SPST switch of an embodiment 3 in accordance with the present invention. The SPST switch shown in FIG. 10 has an input terminal 11a, output terminal 11b, FET 20, capacitor 21 and inductor 22. A second FET switch 14, which consists of a series connection of the FET 20 and capacitor 21, and the inductor 22 connected in parallel with the series connection, has its first terminal connected to the input terminal 11a, and has its second terminal connected to the output terminal 11b.

Here, the drain of the FET 20 can be connected to the input terminal 11a or capacitor 21, and the source of the FET 20 can be connected to the capacitor 21 or input terminal 11a.

Next the operation will be described.

15 In FIG. 10, the FET 20 operates as a switch for switching between the ON state and OFF state by the voltage applied to the gate.

FIG. 11 is an equivalent circuit diagram when the FET 20 in FIG. 10 is brought into the OFF state. As shown in FIG. 11, 20 when the FET 20 is brought into the OFF state, a state arises in which the OFF capacitance 23 and OFF resistance 24 which are connected in parallel are connected in series with the parasitic inductor 25.

When the relationship holds of  $f_2 = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 25) \times (capacitance\ of\ capacitor\ 21)}$  at the 25 used frequency  $f_2$  of the SPST switch in the present embodiment 3, that is, when the capacitor 21 that will cause series resonance with the parasitic inductor 25 is connected, the parasitic inductor 25 that hinders the parallel resonance of the OFF 30 capacitance 23 and inductor 22 is electrically canceled out.

In addition, when the relationship holds of  $f_2 = 1/\sqrt{ } (capacitance of OFF capacitance 23) \times (inductance of inductor 22)$  at the used frequency  $f_2$  of the SPST switch, that is, when the inductor 22 that will cause parallel resonance with the OFF capacitance 23,  
5 the impedance of the output terminal 11b seen from the input terminal 11a becomes high. In this case, the high frequency signal input through the input terminal 11a is not fed to the output terminal 11b. Thus, the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b  
10 is not reduced.

FIG. 12 is an equivalent circuit diagram when the FET 20 in FIG. 10 is brought into the ON state. As shown in FIG. 12, when the FET 20 is brought into the ON state, a state arises in which the ON resistance 26 and the parasitic inductor 25 are  
15 connected in series.

When the relationship holds of  $f_2 = 1/2\pi\sqrt{ } (inductance of parasitic inductor 25) \times (capacitance of capacitor 21)$ , that is, when the capacitor 21 that will cause series resonance with the parasitic inductor 25 is connected, the impedance of the  
20 output terminal 11b seen from the input terminal 11a becomes low. In this case, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal can be reduced.

Here, the inductance of the parasitic inductor 25 in the  
25 OFF state of the FET 20 as shown in FIG. 11 is equal to the inductance of parasitic inductor 25 in the ON state of the FET 20 as shown in FIG. 12. In addition, the values of the capacitance of capacitor 21 that will cause the series resonance with the parasitic inductor 25 in the OFF state and in the ON state of  
30 the FET 20 are equal.

In the present embodiment 3, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which 5 the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the input terminal 11a.

As described above, even when the gate width of the FET 20 is increased to provide the SPST switch with the high 10 withstanding power, the present embodiment 3 offers an advantage of being able to prevent the reduction in the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b, and to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output 15 terminal 11b by connecting the capacitor 21 that will cause the series resonance with the parasitic inductor 25 of the FET 20 at the used frequency  $f_2$  of the SPST switch, and by connecting the inductor 22 that will cause the parallel resonance with the capacitance of the OFF capacitance 23 of the FET 20 at the used 20 frequency.

#### EMBODIMENT 4

FIG. 13 is a circuit diagram showing a configuration of an SPST switch of an embodiment 4 in accordance with the present 25 invention. As the SPST switch of the embodiment 3 as shown in FIG. 10, the SPST switch shown in FIG. 13 has an input terminal 11a, output terminal 11b, FET 20, capacitor 21 and inductor 22. The embodiment 4, however, differs from the embodiment 3 in that the input terminal 11a and the output terminal 11b are connected 30 directly, and in that the second FET switch 14, which consists

of a series connection of the FET 20 and capacitor 21 and the inductor 22 connected in parallel with the series connection, has its first terminal connected to the input terminal 11a and output terminal 11b, and has its second terminal connected to 5 the ground 19.

Here, the drain of the FET 20 can be connected to the input terminal 11a or capacitor 21, and the source of the FET 20 can be connected to the capacitor 21 or input terminal 11a.

Next the operation will be described.

10 In FIG. 13, the FET 20 operates as a switch for switching between the ON state and OFF state by the voltage applied to the gate.

15 FIG. 14 is an equivalent circuit diagram when the FET 20 in FIG. 13 is brought into the OFF state. As shown in FIG. 14, when the FET 20 is brought into the OFF state, a state arises in which the OFF capacitance 23 and OFF resistance 24 which are connected in parallel are connected in series with the parasitic inductor 25.

20 When the relationship holds of  $f_3 = 1/2\pi\sqrt{(\text{inductance of parasitic inductor 25}) \times (\text{capacitance of capacitor 21})}$  at the used frequency  $f_3$  of the SPST switch in the present embodiment, that is, when the capacitor 21 that will cause series resonance with the parasitic inductor 25 of the FET 20 is connected, the parasitic inductor 25 that hinders the parallel resonance of 25 the OFF capacitance 23 and inductor 22 is electrically canceled out. In addition, when the relationship holds of  $f_3 = 1/\sqrt{(\text{capacitance of OFF capacitance 23}) \times (\text{inductance of inductor 22})}$  at the used frequency  $f_3$  of the SPST switch, that is, when the inductor 22 that will cause parallel resonance with the OFF 30 capacitance 23 of the FET 20 is connected, the impedance of the

ground 19 seen from the input terminal 11a becomes high. In this case, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal can be reduced.

5 FIG. 15 is an equivalent circuit diagram when the FET 20 in FIG. 13 is brought into the ON state. As shown in FIG. 15, when the FET 20 is brought into the ON state, a state arises in which the ON resistance 26 and the parasitic inductor 25 are connected in series.

10 When the relationship holds of  $f_3 = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 25) \times (capacitance\ of\ capacitor\ 21)}$ , that is, when the capacitor 21 that will cause series resonance with the parasitic inductor 25 of the FET 20 is connected, the impedance of the ground 19 seen from the input terminal 11a becomes low. In this case, the high frequency signal input through the input terminal 11a propagates to the ground 19 without being fed to the output terminal 11b, and the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b is not reduced.

15 20 Here, the inductance of the parasitic inductor 25 in the OFF state of the FET 20 as shown in FIG. 14 is equal to the inductance of parasitic inductor 25 in the ON state of the FET 20 as shown in FIG. 15. In addition, the values of the capacitance of capacitor 21 that will cause the series resonance with the 25 parasitic inductor 25 in the OFF state and in the ON state of the FET 20 are equal.

20 In the present embodiment 4, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which

the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the input terminal 11a.

As described above, even when the gate width of the FET 20 is increased to provide the SPST switch with the high withstanding power, the present embodiment 4 offers an advantage of being able to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b, and to prevent the reduction in the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b by connecting the capacitor 21 that will cause the series resonance with the parasitic inductor 25 at the used frequency  $f_3$  of the SPST switch, and by connecting the inductor 22 that will cause the parallel resonance with the OFF capacitance 23 at the used frequency.

#### EMBODIMENT 5

FIG. 16 is a circuit diagram showing a configuration of an SPST switch of an embodiment 5 in accordance with the present invention. The SPST switch as shown in FIG. 16, which employs parallel connection of the two second FET switches 14 of the embodiment 3 as shown in FIG. 10, has an input terminal 11a, output terminal 11b, FET 12a, FET 12b, inductor 13a, inductor 13b, capacitor 27a, and capacitor 27b. The second FET switch 25 14a, in which the serial connection of the FET 12a and capacitor 27a is connected in parallel with the inductor 13a, and the second FET switch 14b, in which the serial connection of the FET 12b and capacitor 27b is connected in parallel with the inductor 13b, have their first terminals connected to the input terminal 30 11a and their second terminals connected to the output terminal

11b.

Next the operation will be described.

In FIG. 16, the FET 2a and FET 2b operate as switches for switching between the ON state and OFF state by the voltages applied to the gates.

FIG. 17 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 16 are brought into the OFF state. As shown in FIG. 17, when the FET 12a is brought into the OFF state, a state arises in which the OFF capacitance 15a and OFF resistance 17a which are connected in parallel are connected in series with the parasitic inductor 16a, and when the FET 12b is brought into the OFF state, a state arises in which the OFF capacitance 15b and OFF resistance 17b which are connected in parallel are connected in series with the parasitic inductor 16b.

Here, at the used frequency  $f_4$  of the SPST switch of the present embodiment, it is assumed that the relationship holds of  $f_4 = 1/2\pi\sqrt{(inductance of parasitic inductor 16a) \times (capacitance of capacitor 27a)} = 1/2\pi\sqrt{(inductance of parasitic inductor 16b) \times (capacitance of capacitor 27b)}$ , that is, the capacitor 27a that will cause series resonance with the parasitic inductor 16a is connected to electrically cancel out the parasitic inductor 16a that hinders the parallel resonance of the OFF capacitance 15a and inductor 13a, and the capacitor 27b that will cause series resonance with the parasitic inductor 16b is connected to electrically cancel out the parasitic inductor 16b that hinders the parallel resonance of the OFF capacitance 15b and inductor 13b. In addition, at the used frequency  $f_4$  of the SPST switch, it is assumed that the relationship holds of  $f_4 = 1/\sqrt{(capacitance of OFF capacitance 15a) \times (inductance of inductor 13a)} = 1/\sqrt{(capacitance of OFF$

capacitance 15b)  $\times$  (inductance of inductor 13b), that is, the inductor 13a that will cause parallel resonance with the OFF capacitance 15a is connected, and the inductor 13b that will cause parallel resonance with the OFF capacitance 15b is connected. In this case, the impedance of the output terminal 11b seen from the input terminal 11a becomes high. Thus, the high frequency signal input through the input terminal 11a is not fed to the output terminal 11b, and the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b is not reduced.

FIG. 18 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 16 are brought into the ON state. As shown in FIG. 18, when the FET 12a is brought into the ON state, a state arises in which the ON resistance 18a and parasitic inductor 16a are connected in series, and when the FET 12b is brought into the ON state, a state arises in which the ON resistance 18b and parasitic inductor 16b are connected in series.

Here, at the used frequency  $f_4$  of the SPST switch, it is assumed that the relationship holds of  $f_4 = 1/2\pi\sqrt{(inductance of parasitic inductor 16a) \times (capacitance of capacitor 27a)} = 1/2\pi\sqrt{(inductance of parasitic inductor 16b) \times (capacitance of capacitor 27b)}$ , that is, the capacitor 27a that will cause series resonance with the parasitic inductor 16a is connected, and the capacitor 27b that will cause series resonance with the parasitic inductor 16b is connected. In this case, the impedance of the output terminal 11b seen from the input terminal 11a becomes low. Thus, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal can be reduced.

Here, the inductance of the parasitic inductors 16a and 16b in the OFF state of the FETs 12a and 12b shown in FIG. 17 is equal to the inductance of the parasitic inductors 16a and 16b in the ON state of the FETs 12a and 12b shown in FIG. 18.

5 In addition, the values of the capacitances of the capacitors 27a and 27b that will cause the series resonance with the parasitic inductors 16a and 16b in the OFF state and in the ON state of the FETs 12a and 12b are equal.

In the present embodiment 5, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the 15 input terminal 11a.

In addition, although the two second FET switches 14a and 14b are connected in parallel in the present embodiment 5, two or more second FET switches can be connected in parallel.

As described above, even when the gate width of the FETs 20 12a and 12b is increased to provide the SPST switch with the high withstanding power, the present embodiment 5 offers an advantage of being able to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b without reducing the isolation of the high frequency 25 signal from the input terminal 11a to the output terminal 11b by connecting the capacitor 27a that will cause the series resonance with the parasitic inductor 16a at the used frequency  $f_4$  of the SPST switch, by connecting the capacitor 27b that will cause the series resonance with the parasitic inductor 16b, by 30 connecting the inductor 13a that will cause the parallel

resonance with the OFF capacitance 15a, and by connecting the inductor 13b that will cause the parallel resonance with the OFF capacitance 15b.

5 EMBODIMENT 6

FIG. 19 is a circuit diagram showing a configuration of an SPST switch of an embodiment 6 in accordance with the present invention. The SPST switch as shown in FIG. 19, which employs parallel connection of the two second FET switches 14 of the 10 embodiment 4 as shown in FIG. 13, has an input terminal 11a, output terminal 11b, FET 12a, FET 12b, inductor 13a, inductor 13b, capacitor 27a, capacitor 27b, and ground 19. The second FET switch 14a, in which the serial connection of the FET 12a and capacitor 27a is connected in parallel with the inductor 15 13a, and the second FET switch 14b, in which the serial connection of the FET 12b and capacitor 27b is connected in parallel with the inductor 13b, have their first terminals connected to the input terminal 11a and output terminal 11b, and their second terminals connected to the ground 19.

20 Next the operation will be described.

In FIG. 19, the FET 2a and FET 2b operate as switches for switching between the ON state and OFF state by the voltages applied to the gates.

FIG. 20 is an equivalent circuit diagram when the FET 12a 25 and FET 12b in FIG. 19 are brought into the OFF state. As shown in FIG. 20, when the FET 12a is brought into the OFF state, a state arises in which the OFF capacitance 15a and OFF resistance 17a which are connected in parallel are connected in series with the parasitic inductor 16a, and when the FET 12b is brought into 30 the OFF state, a state arises in which the OFF capacitance 15b

and OFF resistance 17b which are connected in parallel are connected in series with the parasitic inductor 16b.

Here, at the used frequency  $f_4$  of the SPST switch of the present embodiment, it is assumed that the relationship holds of  $f_4 = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 16a) \times (capacitance\ of\ capacitor\ 27a)} = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 16b) \times (capacitance\ of\ capacitor\ 27b)}$ , that is, the capacitor 27a that will cause series resonance with the parasitic inductor 16a is connected to electrically cancel out the parasitic inductor 16a that hinders the parallel resonance of the OFF capacitance 15a and inductor 13a, and the capacitor 27b that will cause series resonance with the parasitic inductor 16b is connected to electrically cancel out the parasitic inductor 16b that hinders the parallel resonance of the OFF capacitance 15b and inductor 13b. In addition, at the used frequency  $f_4$  of the SPST switch, it is assumed that the relationship holds of  $f_4 = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 15a) \times (inductance\ of\ inductor\ 13a)} = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 15b) \times (inductance\ of\ inductor\ 13b)}$ , that is, the inductor 13a that will cause parallel resonance with the OFF capacitance 15a is connected, and the inductor 13b that will cause parallel resonance with the OFF capacitance 15b is connected. In this case, the impedance of the ground 19 seen from the input terminal 11a becomes high. Thus, the high frequency signal input through the input terminal 11a is fed to the output terminal 11b, and the propagation loss of the high frequency signal can be reduced.

FIG. 21 is an equivalent circuit diagram when the FET 12a and FET 12b in FIG. 19 are brought into the ON state. As shown in FIG. 21, when the FET 12a is brought into the ON state, a

state arises in which the ON resistance 18a and parasitic inductor 16a are connected in series, and when the FET 12b is brought into the ON state, a state arises in which the ON resistance 18b and parasitic inductor 16b are connected in series.

Here, at the used frequency  $f_4$  of the SPST switch, it is assumed that the relationship holds of  $f_4 = 1/2\pi\sqrt{(inductance of parasitic inductor 16a) \times (capacitance of capacitor 27a)} = 1/2\pi\sqrt{(inductance of parasitic inductor 16b) \times (capacitance of capacitor 27b)}$ , that is, the capacitor 27a that will cause series resonance with the parasitic inductor 16a is connected, and the capacitor 27b that will cause series resonance with the parasitic inductor 16b is connected. In this case, the impedance of the output terminal 11b seen from the input terminal 11a becomes low. Thus, the high frequency signal input through the input terminal 11a is not fed to the output terminal 11b, and the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b is not reduced.

Here, the inductance of the parasitic inductors 16a and 16b in the OFF state of the FETs 12a and 12b shown in FIG. 20 is equal to the inductance of the parasitic inductors 16a and 16b in the ON state of the FETs 12a and 12b shown in FIG. 21. In addition, the values of the capacitances of the capacitors 27a and 27b that will cause the series resonance with the parasitic inductors 16a and 16b in the OFF state and in the ON state of the FETs 12a and 12b are equal.

In the present embodiment 6, although the high frequency signal is controlled in such a manner that it is input through the input terminal 11a and is fed to the output terminal 11b, this is not essential. A configuration is also possible in which

the high frequency signal is controlled in such a manner that it is input through the output terminal 11b and is fed to the input terminal 11a.

In addition, although the two second FET switches 14a and 5 14b are connected in parallel in the present embodiment 6, two or more second FET switches can be connected in parallel.

As described above, even when the gate width of the FETs 12a and 12b is increased to provide the SPST switch with the high withstanding power, the present embodiment 6 offers an 10 advantage of being able to reduce the propagation loss of the high frequency signal from the input terminal 11a to the output terminal 11b, and to prevent the reduction in the isolation of the high frequency signal from the input terminal 11a to the output terminal 11b by connecting the capacitor 27a that will 15 cause the series resonance with the parasitic inductor 16a at the used frequency  $f_4$  of the SPST switch, by connecting the capacitor 27b that will cause the series resonance with the parasitic inductor 16b, by connecting the inductor 13a that will cause the parallel resonance with the OFF capacitance 15a, and 20 by connecting the inductor 13b that will cause the parallel resonance with the OFF capacitance 15b.

#### EMBODIMENT 7

FIG. 22 is a circuit diagram showing a configuration of 25 an SPDT switch of an embodiment 7 in accordance with the present invention. The SPDT switch as shown in FIG. 22 includes an input terminal 28a, output terminal 28b, output terminal 28c, FET 29a, FET 29b, FET 29c, inductor 30a, inductor 30b, inductor 30c, capacitor 32, line 33 and ground 19. A first FET switch 31a, 30 in which the FET 29a and inductor 30a are connected in parallel,

and a first FET switch 31b, in which the FET 29b and inductor 30b are connected in parallel, have their first terminals connected to the input terminal 28a, and their second terminals connected to the output terminal 28c. The line 33 has its first 5 terminal connected to the input terminal 28a, and its second terminal connected to the output terminal 28b. A second FET switch 31c, in which a series connection of the FET 29c and capacitor 32 is connected in parallel with the inductor 30c, has its first terminal connected to the output terminal 28b, 10 and its second terminal connected to the ground 19. Here, the line length of the line 33 is assumed to be 1/4 wavelength at a used frequency  $f_5$ .

In the present embodiment 7, the first FET switches 14a and 14b as shown in FIG. 4 of the embodiment 1 are used as the 15 first FET switches 31a and 31b, and the second FET switch 14 as shown in FIG. 13 of the embodiment 4 is used as the second FET switch 31c.

Next the operation will be described.

In FIG. 22, the FET 29a, FET 29b and FET 29c operate as 20 switches for switching between the ON state and OFF state by the voltages applied to the gates.

FIG. 23 is an equivalent circuit diagram when the FET 29a, FET 29b and FET 29c in FIG. 22 are brought into the OFF state. As shown in FIG. 23, when the FET 29a is brought into the OFF 25 state, a state arises in which the OFF capacitance 34a and OFF resistance 35a which are connected in parallel are connected in series with the parasitic inductor 36a, when the FET 29b is brought into the OFF state, a state arises in which the OFF capacitance 34b and OFF resistance 35b which are connected in parallel are connected in series with the parasitic inductor 36b, and when the FET 29c is brought into the OFF state, a state arises in which the OFF capacitance 34c and OFF resistance 35c which are connected in parallel are connected in series with the parasitic inductor 36c.

36b, and when the FET 29c is brought into the OFF state, a state arises in which the OFF capacitance 34c and OFF resistance 35c which are connected in parallel are connected in series with the parasitic inductor 36c.

5 It is assumed here that at the used frequency  $f_5$  of the SPDT switch of the present embodiment, the relationships hold of  $f_5 = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 36c) \times (capacitance\ of\ capacitor\ 32)}$ , and  $f_5 = 1/2\pi\sqrt{(capacitance\ of\ OFF\ capacitance\ 34c) \times (inductance\ of\ inductor\ 30c)}$ .

10 15 Connecting the two FETs 29a and 29b in parallel can halve their individual gate width to achieve the same withstand ing power. Halving the individual gate width can make the reactance components of the parasitic inductors 36a and 36b of the FETs 29a and FET 29b small enough as compared with the reactance components of the OFF capacitances 34a and 34b at the frequency  $f_5$  used by the SPDT switch, and make the OFF resistances 35a and 35b large enough.

20 In addition, at the used frequency  $f_5$  of the SPDT switch, when the relationship holds of  $f_5 = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 34a) \times (inductance\ of\ inductor\ 30a)} = 1/\sqrt{(capacitance\ of\ OFF\ capacitance\ 34b) \times (inductance\ of\ inductor\ 30b)}$ , the impedance of the output terminal 28b seen from the input terminal 28a becomes low, and the impedance of the output terminal 28c seen from the input terminal 28a becomes high. In 25 this case, the high frequency signal input through the input terminal 28a is fed to the output terminal 28b, and the propagation loss of the high frequency signal can be reduced. In contrast, the high frequency signal input through the input terminal 28a is not fed to the output terminal 28c, and the 30 isolation of the high frequency signal from the input terminal

28a to the output terminal 28C is not reduced.

FIG. 24 is an equivalent circuit diagram when the FET 29a, FET 29b and FET 29c in FIG. 22 are brought into the ON state. As shown in FIG. 24, when the FET 29a is brought into the ON state, a state arises in which the ON resistance 37a and parasitic inductor 36a are connected in series, when the FET 29b is brought into the ON state, the ON resistance 37b and parasitic inductor 36b are connected in series, and when the FET 29c is brought into the ON state, the ON resistance 37c and parasitic inductor 36c are connected in series.

It is assumed here that at the used frequency  $f_5$  of the SPDT switch, the relationship holds of  $f_5 = 1/2\pi\sqrt{(inductance\ of\ parasitic\ inductor\ 36c) \times (capacitance\ of\ capacitor\ 32)}$ . Since the line length of the line 33 is 1/4 wavelength at the used frequency  $f_5$ , the impedance of the output terminal 28b seen from the input terminal 28a becomes high. In addition, since the first FET switches 31a and 31b are connected in parallel, the impedance of the output terminal 28c seen from the input terminal 28a becomes low. In this case, the high frequency signal input through the input terminal 28a is fed to the output terminal 28c, and the propagation loss of the high frequency signal can be reduced. At the same time, the high frequency signal input through the input terminal 28a is not fed to the output terminal 28b, and the isolation of the high frequency signal from the input terminal 28a to the output terminal 28b is not reduced.

Although the SPDT switch in the present embodiment 7 employs the first FET switches 31a and 31b and second FET switch 31c, the SPDT switch can be constructed from the first FET switches shown in the embodiments 1 and 2, or from the second FET switches shown in the embodiments 3, 4, 5, and 6, or from an appropriate

combination of the first FET switches and second FET switches as shown in the embodiments 1-6.

As described above, the present embodiment 7 enables the SPDT switch to be constructed by combining the SPST switch from the embodiment 1 to the embodiment 6, thereby offering an advantage of being able to reduce the propagation loss of the high frequency signal from the input terminal 28a to the output terminal 28b or 28c, and to prevent the reduction in the isolation of the high frequency signal from the input terminal 28a to the output terminal 28b or 28c.

#### EMBODIMENT 8

FIG. 25 is a circuit diagram showing a configuration of an MPMT switch of an embodiment 8 in accordance with the present invention. Although only the SPDT switch is described in connection with FIG. 22 of the foregoing embodiment 7, combining the SPST switches from the foregoing embodiment 1 to embodiment 6 can construct an MPMT switch as shown in FIG. 25, for example.

The MPMT switch as shown in FIG. 25 includes input terminals or output terminals 38a, 38b, 38c and 38d; FETs 39a, 39b, 39c and 39d; capacitors 40a, 40b, 40c and 40d; and inductors 41a, 41b, 41c and 41d. The FET 39a, capacitor 40a and inductor 41a constitute a second FET switch 42a; the FET 39b, capacitor 40b and inductor 41b constitute a second FET switch 42b; the FET 39c, capacitor 40c and inductor 41c constitute a second FET switch 42c; and the FET 39d, capacitor 40d and inductor 41d constitute a second FET switch 42d.

The second FET switches 42a, 42b, 42c and 42d have their first terminals connected to the input terminals or output terminals 38a, 38b, 38c and 38d, respectively, and their second

terminals connected with each other.

Next the operation will be described.

FIG. 26 is a table illustrating the operation of the MPMT switch of FIG. 25. Controlling the turning on and off of the 5 individual FETs 39a, 39b, 39c and 39d enables the high frequency signal input through a designate input terminal to be fed to a designated output terminal.

Although the MPMT switch in the present embodiment 8 employs the second FET switches 42a, 42b, 42c and 42d, the MPMT switch 10 can be constructed from the first FET switches as shown in the embodiment 1 or 2, or from the second FET switches as shown in the embodiment 3, 4, 5 or 6, or from an appropriate combination of the first FET switches and second FET switches as shown in the embodiments 1-6.

15 As described above, the present embodiment 8 can configure the MPMT switch by combining the SPST switches shown from the embodiment 1 to embodiment 6, thereby offering an advantage of being able to reduce the propagation loss of the high frequency signal from the input terminal to the output terminal, and to 20 prevent the reduction in the isolation of the high frequency signal from the input terminal to the output terminal.

#### INDUSTRIAL APPLICABILITY

As described above, the SPST switch, SPDT switch and MPMT 25 switch in accordance with the present invention can reduce the propagation loss of the high frequency signal, and prevent the reduction of the isolation of the high frequency signal.